

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claims 1-27: cancelled.

28. (new) A CMOS inverter comprising a substrate including a strained layer thereon, a pMOSFET and an nMOSFET each having a channel through the strained layer.

29. (new) The CMOS inverter of claim 28 further comprising a relaxed layer between the substrate and the strained layer, wherein the relaxed layer induces strain within the strained layer.

30. (new) The CMOS inverter of claim 28 further comprising a planarized surface between the strained layer and the substrate.

31. (new) The CMOS inverter of claim 28, wherein the strained layer has a surface roughness of less than about 1nm.

32. (new) The CMOS inverter of claim 28 further comprising an oxide layer disposed beneath the strained layer.

33. (new) The CMOS inverter of claim 29 further comprising a graded buffer layer between the relaxed layer and the substrate.

34. (new) The CMOS inverter of claim 28, wherein a ratio of gate width of the pMOSFET to gate width of the nMOSFET is approximately equal to a ratio of electron mobility to hole mobility in the strained layer.

35. (new) The CMOS inverter of claim 28, wherein a ratio of gate width of the pMOSFET to gate width of the nMOSFET is approximately equal to the square root of a ratio of electron mobility to the hole mobility in the strained layer.

36. (new) The CMOS inverter of claim 28, wherein a reduced gate drive is used to lower power consumption.

37. (new) An integrated circuit comprising:

a heterostructure including a substrate and a strained layer thereon; and

a p transistor and an n transistor formed in the heterostructure, transistors each having a channel through the strained layer and being interconnected in a CMOS circuit.

38. (new) The integrated circuit of claim 37, wherein the heterostructure further comprises a relaxed layer between the substrate and the strained layer, wherein the relaxed layer induces strain within the strained layer.

39. (new) The integrated circuit of claim 37, wherein the heterostructure further comprises a planarized surface between the strained layer and the substrate.

40. (new) The integrated circuit of claim 37, wherein the strained layer has a surface roughness of less than about 1nm.

41. (new) The integrated circuit of claim 37, wherein the heterostructure further comprises an oxide layer disposed beneath the strained layer.

42. (new) The integrated circuit of claim 38, wherein the heterostructure further comprises a graded buffer layer between the relaxed layer and the substrate.
43. (new) The integrated circuit of claim 37, wherein the CMOS circuit comprises a logic gate.
44. (new) The integrated circuit of claim 37, wherein the CMOS circuit comprises a NOR gate.
45. (new) The integrated circuit of claim 37, wherein the CMOS circuit comprises an XOR gate.
46. (new) The integrated circuit of claim 37, wherein the CMOS circuit comprises a NAND gate.
47. (new) The integrated circuit of claim 37, wherein the p-channel transistor serves as a pull-up transistor in the CMOS circuit and the n-channel transistor serves as a pull-down transistor in the CMOS circuit.
48. (new) The integrated circuit of claim 37, wherein the CMOS circuit comprises an inverter.